PATENT ABSTRACTS OF JAPAN

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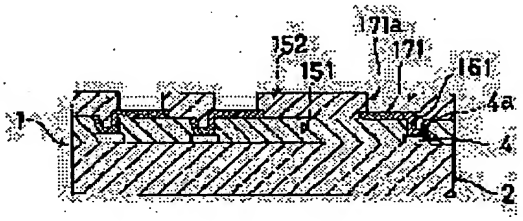
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PURPOSE: To provide the semiconductor device, which can be manufactured as the high-quality product in excellent productivity even if the number of semiconductor elements becomes many, the electrodes of the semiconductor elements are made small and the electrode pitch is narrowed.
CONSTITUTION: This device has the following parts. A semiconductor element 2 has a plurality of element electrodes 4, wherein integrated circuits are formed. A first insulating layer 151 is formed on the surface of the semiconductor element 2. A plurality of external electrodes 171 are formed on the first insulating layer 151. A first wiring part 161 connects the external electrode 171 and the element electrodes 4 electrically. The first conducint layers comprising these parts are provided.



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CLAIMS

[Claim(s)]

[Claim 1] The semiconductor device characterized by having the 1st conductive layer which consists of the 1st wiring which connects electrically two or more external electrodes formed on the semiconductor device which an integrated circuit is formed and has two or more component electrodes, the 1st insulating layer formed in the front face of said semiconductor device, and said 1st insulating layer, and said external electrode and said component electrode.

[Claim 2] The semiconductor device which an integrated circuit is formed and has two or more component electrodes, and the 1st insulating layer formed in the front face of said semiconductor device, The 1st conductive layer which consists of the 1st wiring which was formed on said 1st insulating layer and was electrically connected with said component electrode, The semiconductor device characterized by having the 2nd conductive layer which consists of the 2nd wiring which connects electrically the 2nd insulating layer formed on said 1st conductive layer, two or more external electrodes formed on said 2nd insulating layer, and said external electrode and said 1st wiring, or said component electrode.

[Claim 3] The semiconductor device according to claim 2 with which the external electrode which has the multilayer-interconnection structure where the insulating layer and the conductive layer were repeatedly formed on the surface of the semiconductor device, and was electrically connected with the component electrode of said semiconductor device through said multilayer-interconnection structure is formed in the maximum front face.

[Claim 4] The coefficient of thermal expansion of the insulating material of an insulating layer is a semiconductor device according to claim 1, 2, or 3 which is the middle value of the coefficient of thermal expansion of a semiconductor device, and the coefficient of thermal expansion of the circuit board.

[Claim 5] The insulating material of an insulating layer is a semiconductor device according to claim 1, 2, 3, or 4 which is a photosensitive epoxy resin.

[Claim 6] Form the insulating layer by the photosensitive insulating material in the front face of the semiconductor device which an integrated circuit is formed and has two or more component electrodes, and negatives are exposed and developed using a mask. The 1st insulation layer forming process which prepares the 1st insulating layer which has a through tube to said component electrode, The manufacture approach of the semiconductor device characterized by having the 1st conductive layer formation process which prepares the 1st conductive layer which consists of the 1st wiring which forms the conductive layer by the conductive ingredient on said 1st insulating layer, operates orthopedically, and connects electrically an external electrode, and two or more of said external electrodes and said component electrodes.

[Claim 7] Form the insulating layer by the photosensitive insulating material in the front face of the semiconductor device which an integrated circuit is formed and has two or more component electrodes, and negatives are exposed and developed using a mask. The 1st insulation layer forming process which prepares the 1st insulating layer which has a through tube to said component electrode, The 1st conductive layer formation process which prepares the 1st conductive layer which has the 1st wiring

which forms the conductive layer by the conductive ingredient on said 1st insulating layer, operates orthopedically, and is connected to said component electrode, Form the insulating layer by the photosensitive insulating material on said 1st conductive layer, and negatives are exposed and developed using a mask. The 2nd insulation layer forming process which prepares the 2nd insulating layer which has a through tube to said 1st wiring, The conductive layer by the conductive ingredient is formed on said 2nd insulating layer, and it operates orthopedically. Two or more external electrodes, The manufacture approach of the semiconductor device characterized by having the 2nd conductive layer formation process which prepares the 2nd conductive layer which consists of the 2nd wiring which connects electrically said external electrode and said 1st wiring, or said component electrode.

[Claim 8] The manufacture approach of a semiconductor device according to claim 7 of repeating an insulation layer forming process and a conductive layer formation process on the surface of a semiconductor device, establishing multilayer-interconnection structure, and preparing the external electrode electrically connected with the component electrode of a semiconductor device through said multilayer-interconnection structure in the maximum front face.

[Claim 9] The manufacture approach of a semiconductor device according to claim 6, 7, or 8 of giving an insulation layer forming process and a conductive layer formation process to two or more semiconductor devices of the condition of a wafer.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the semiconductor device which mounted the semiconductor device in high density at the semi-conductor carrier, and its manufacture approach.

[0002]

[Description of the Prior Art] The conventional semiconductor device mounted in high density is explained to the circuit board based on drawing 5 - drawing 8 .

[0003] It has connected with the circuit board 12, once connecting with the semi-conductor carrier 3 and using a semiconductor device 2 as a semiconductor device 1 from the former, as shown in drawing 6 when it mounts a semiconductor device 2 in the circuit board 12. There are the following two reasons in this.

[0004] With a raise in basic wages semiconductor device, a blemish tends to be attached and inspection of the 1st reason is impossible before mounting. Therefore, in order to enable it to inspect before mounting and to prevent property degradation by humidity, the semi-conductor carrier 3 is equipped with a semiconductor device 2, and restoration covering of the circumference is carried out with the encapsulant 7 of epoxy system resin.

[0005].As for the 2nd reason, a bias tooth space is constitutionally restricted for a component electrode location to the periphery of a raise in basic wages semiconductor device, these component electrodes 4 with which the tooth space was restricted are small, and, as for a raise in basic wages semiconductor device, its inter-electrode distance is narrow. Therefore, it is difficult to connect said component electrode 4 to the substrate electrode 11 of the circuit board 12 directly.
[0006] In order to make this connection easy, arrangement of the component lateral electrode 6 of one side is suitable for connection with the component electrode 4 of a semiconductor device 2, and arrangement of the substrate lateral electrode 8 of an opposite side connects a semiconductor device 2 to said one side of the semi-conductor carrier 3 suitable for connection with the substrate electrode 11 of the circuit board 12, and is carrying out restoration covering of that circumference with the encapsulant 7 of epoxy system resin by the aforementioned reason.
[0007] Therefore, in the 1st conventional example, in drawing 6 , a semiconductor device 1 forms the golden bump 5 on it, connects the component electrode 4 of a semiconductor device 2 to the component lateral electrode 6 of the semi-conductor carrier 3 with cream solder or electroconductive glue, and carries out restoration covering of the clearance between the connected semiconductor device 2 and the semi-conductor carrier 3, and the connected periphery of a semiconductor device 2 with the encapsulant 7 of epoxy system resin. And it connects electrically between said component lateral electrodes 6 and said substrate lateral electrodes 8.
[0008] In connecting a semiconductor device 1 to the circuit board 12, as first shown in drawing 6 , a bump 9 is formed in said substrate lateral electrode 8 of the semi-conductor carrier 3, and it prints the cream solder 13 to the substrate electrode 11 of the circuit board 12.
[0009] Subsequently, as shown in drawing 7 , the substrate lateral electrode 8 of a semiconductor device 1 is positioned, laid and heated on the substrate electrode 11 of the circuit board 12, melting and hardening of said applied cream solder 13 are done, and the substrate lateral electrode 8 is connected to the substrate electrode 11.
[0010] Next, the 2nd conventional example is explained based on drawing 8 .
[0011] In drawing 8 , a semiconductor device 1 forms the golden bump 5 on two or more component electrodes 4 of a semiconductor device 2, and connects the bump 5 of said gold to the component lateral electrode 6 formed on the polyimide film 14 of electroconductive glue 5a, and the gap of a semiconductor device 2 and a polyimide film 14 is filled up with the encapsulant 7 of epoxy system resin. And a bump 9 is formed in the component lateral electrode 6, and this is connected to the electrode of the circuit board. Although drawing 8 shows a cross section, in fact, it is arranged at space perpendicularly densely [the component electrode 4 of a large number which incline toward the periphery of a semiconductor device 2], and the component lateral electrode 6 is arranged in the shape of a grid to the tooth space where the center section of the semiconductor device 2 is large.
[0012]
[Problem(s) to be Solved by the Invention] However, as shown in drawing 5 , a process until it ships as a semiconductor device from the wafer of a semiconductor device needs to divide the wafer of a semiconductor device into each semiconductor device at a division process, and needs to repeat bump formation of only the number of the component electrodes to each semiconductor device with a bump formation process, and it is necessary to do positioning and junction of the semiconductor devices which bump formation ended at positioning / junction process one by one with the configuration of the above-mentioned conventional example, at a semi-conductor carrier.
[0013] Therefore, when the number of the component electrodes of a semiconductor device increases like recently, there is a trouble that a production process takes time amount very much.
[0014] Moreover, there is a trouble that the hardening process of the encapsulant 7 shown in drawing 6 and drawing 7 also takes a long time.
[0015] As a property for which the semi-conductor carrier 3 is asked, moreover, the display flatness In order to maintain the dependability of electrode bonding strength, the amount of curvatures of the

magnitude of 10 micrometers or less and a substrate lateral electrode is more than 100micrometerx100micrometer. If the amount of curvatures exceeds 10 micrometers, poor electrode junction will occur, and if the area of a substrate lateral electrode runs short or a pitch becomes narrow too much, manufacture of high quality will become difficult, and there is a trouble that the defect of a bridge etc. occurs.

[0016] This invention makes it a technical problem to offer the semiconductor device which can manufacture the product of high quality with sufficient productivity, and its manufacture approach, even if solve the above-mentioned trouble, the number of component electrodes of a semiconductor device increases, the component electrode of a semiconductor device becomes small and an electrode pitch becomes narrow.

[0017]

[Means for Solving the Problem] The semiconductor device of the 1st invention of this application is characterized by having the 1st conductive layer which consists of the 1st wiring which connects electrically two or more external electrodes formed on the semiconductor device which an integrated circuit is formed and has two or more component electrodes, the 1st insulating layer formed in the front face of said semiconductor device, and said 1st insulating layer, and said external electrode and said component electrode, in order to solve the above-mentioned technical problem.

[0018] The semiconductor device which an integrated circuit is formed and has two or more component electrodes in order that the semiconductor device of the 2nd invention of this application may solve the above-mentioned technical problem, The 1st insulating layer formed in the front face of said semiconductor device, and the 1st conductive layer which consists of the 1st wiring which was formed on said 1st insulating layer and was electrically connected with said component electrode, It is characterized by having the 2nd conductive layer which consists of the 2nd wiring which connects electrically the 2nd insulating layer formed on said 1st conductive layer, two or more external electrodes formed on said 2nd insulating layer, and said external electrode and said 1st wiring, or said component electrode.

[0019] Moreover, in order to solve the above-mentioned technical problem, it is suitable for the semiconductor device of the 2nd invention of this application that the external electrode which has the multilayer-interconnection structure where the insulating layer and the conductive layer were repeatedly formed on the surface of the semiconductor device, and was electrically connected with the component electrode of said semiconductor device through said multilayer-interconnection structure is formed in the maximum front face.

[0020] Moreover, in order that the semiconductor device of the 1st, 2nd, or 3rd invention of this application may solve the above-mentioned technical problem, it is suitable for the coefficient of thermal expansion of the insulating material of an insulating layer that it is the middle value of the coefficient of thermal expansion of a semiconductor device and the coefficient of thermal expansion of the circuit board.

[0021] Moreover, in order to solve the above-mentioned technical problem, as for the semiconductor device of the 1st, 2nd, 3rd, or 4th invention of this application, it is suitable for the insulating material of an insulating layer that it is a photosensitive epoxy resin.

[0022] In order that the manufacture approach of the semiconductor device the 3rd invention of this application may solve the above-mentioned technical problem Form the insulating layer by the photosensitive insulating material in the front face of the semiconductor device which an integrated circuit is formed and has two or more component electrodes, and negatives are exposed and developed using a mask. The 1st insulation layer forming process which prepares the 1st insulating layer which has a through tube to said component electrode, It is characterized by having the 1st conductive layer formation process which prepares the 1st conductive layer which consists of the 1st wiring which forms the conductive layer by the conductive ingredient on said 1st insulating layer, operates orthopedically, and connects electrically an external electrode, and two or more of said external electrodes and said

component electrodes.
[0023] In order that the manufacture approach of the semiconductor device the 4th invention of this application may solve the above-mentioned technical problem Form the insulating layer by the photosensitive insulating material in the front face of the semiconductor device which an integrated circuit is formed and has two or more component electrodes, and negatives are exposed and developed using a mask. The 1st insulation layer forming process which prepares the 1st insulating layer which has a through tube to said component electrode, The 1st conductive layer formation process which prepares the 1st conductive layer which has the 1st wiring which forms the conductive layer by the conductive ingredient on said 1st insulating layer, operates orthopedically, and is connected to said component electrode, Form the insulating layer by the photosensitive insulating material on said 1st conductive layer, and negatives are exposed and developed using a mask. The 2nd insulation layer forming process which prepares the 2nd insulating layer which has a through tube to said 1st wiring, It is characterized by having the 2nd conductive layer formation process which prepares the 2nd conductive layer which consists of the 2nd wiring which forms the conductive layer by the conductive ingredient on said 2nd insulating layer, operates orthopedically, and connects electrically two or more external electrodes, and said external electrode and said 1st wiring, or said component electrode.
[0024] Moreover, in order to solve the above-mentioned technical problem, it is suitable for the manufacture approach of the semiconductor device the 4th invention of this application to repeat an insulation layer forming process and a conductive layer formation process on the surface of a semiconductor device, to establish multilayer-interconnection structure, and to prepare the external electrode electrically connected with the component electrode of a semiconductor device through said multilayer-interconnection structure on the maximum front face.
[0025] Moreover, in order to solve the above-mentioned technical problem, it is suitable for the manufacture approach of the semiconductor device the 3rd or 4th invention of this application to two or more semiconductor devices of the condition of a wafer to give an insulation layer forming process and a conductive layer formation process.
[0026]
[Function] The manufacture approach of the semiconductor device of the invention in this application, and the semiconductor device of the invention in this application Form the insulating layer by the photosensitive insulating material in the front face of the semiconductor device which an integrated circuit is formed and has two or more component electrodes, and negatives are exposed and developed using a mask. The 1st insulation layer forming process which prepares the 1st insulating layer which has a through tube to said component electrode, It is what is depended on combination with the 1st conductive layer formation process which prepares the 1st conductive layer which has the 1st wiring which forms the conductive layer by the conductive ingredient on said 1st insulating layer, operates orthopedically, and is connected to said component electrode. Since these processes can use the track record of the manufacturing technology of a semiconductor device, a quality semiconductor device can be obtained corresponding to the component electrode of the semiconductor device made [overly] detailed, or its pitch.
[0027] Moreover, since the process of the conventional technique which requires the time amount of attaching a bump for every component electrode of a semiconductor device is lost, it bundles up for every semiconductor device, it bundles up for every wafer further and a component electrode and external inter-electrode electrode junction is performed, productivity can be improved very greatly.
[0028] Moreover, by using the insulating material which has the middle coefficient of thermal expansion of the coefficient of thermal expansion of a semiconductor device, and the coefficient of thermal expansion of the circuit board in the insulating material to be used, the thermal stress generated according to the difference of thermal expansion is eased, and dependability can be improved.
[0029]
[Example] The 1st example of the semiconductor device of this invention is explained based on drawing

1 and drawing 2 R> 2.
[0030] In drawing 1 and drawing 2 , the 1st insulating layer 151 is formed on the semiconductor device 2 in which the structure of the semiconductor device 1 of this example has two or more component electrodes 4, and through tube 4a is prepared on the component electrode 4. On the 1st insulating layer 151, the 1st wiring 161 and the 1st external electrode 171 were formed, and the 1st wiring 161 has connected the 1st external electrode 171 and the component electrode 4. The 2nd insulating layer 152 was formed on the 1st insulating layer 151, the 1st wiring 161, and the 1st external electrode 171, and through tube 171a has opened on the 1st external electrode 171. This 1st external electrode 171 turns into an external electrode of the semiconductor device 1 of this example.
[0031] And although the area of the component electrode 4 will become small and an inter-electrode pitch will become narrow if a semiconductor device 2 is miniaturized and the number of the component electrodes 4 increases since it inclines toward the periphery of a semiconductor device 2 and is arranged by the configuration of a semiconductor device 2 as the component electrode 4 is shown in drawing 2 The 1st external electrode 171 is arranged to the tooth space where the center section of the semiconductor device 2 is large, there are few limits of a form, area, and arrangement, and as shown in drawing 2 , it can be freely designed to the arrangement which is easy to connect to the substrate electrode of the circuit board at arrangement of the shape for example, of a grid etc.
[0032] The 2nd example of the semiconductor device of this invention is explained based on drawing 3 .
[0033] In drawing 3 , the structure of semiconductor device 1a of this example makes structure of the 1st example multilayer structure.
[0034] The 1st insulating layer 151 is formed on the semiconductor device 2 which has two or more component electrodes 4, and through tube 4a is prepared on the component electrode 4.
[0035] On the 1st insulating layer 151, the 1st wiring 161 and 1st connection electrode 161a were prepared, and the 1st wiring 161 is connected to the component electrode 4 and 1st connection electrode 161a.
[0036] The 2nd insulating layer 152 is formed on the 1st insulating layer 151, the 1st wiring 161, and 1st connection electrode 161a, and through tube 161b is prepared on 1st connection electrode 161a.
[0037] On the 2nd insulating layer 152, the 2nd wiring 162 and the 2nd external electrode 172 were formed, and the 2nd wiring 162 is connected to 1st connection electrode 161a.
[0038] The 3rd insulating layer 153 is formed on the 2nd insulating layer 152, the 2nd wiring 162, and the 2nd external electrode 172, and through tube 172a is prepared on the 2nd external electrode 172.
[0039] The above-mentioned multilayer structure is possible and can design any number of layers [not only two-layer but] addition of circuit elements, such as resistance and capacity, in the wiring section of these layers.
[0040] The manufacture approach of the semiconductor device of this invention is explained based on drawing 4 and drawing 5 R> 5.
[0041] In drawing 4 , 1st insulating-layer 151a is first formed in the front face of the semiconductor device 2 which has the component electrode 4 with the 1st insulation layer forming process by the photosensitive insulating material. As for a photosensitive insulating material, it is desirable that it is epoxy system resin. Formation of 1st insulating-layer 151a may print a liquefied thing, and may make a film-like thing adhere.
[0042] Next, it takes exposure 18 at an exposure process using the mask 17 formed so that the light of a predetermined pattern might pass.
[0043] Next, at a development process, by developing negatives, through tube 4a is prepared on the component electrode 4, and the 1st insulating layer 151 is formed.
[0044] Next, 1st conductive ingredient layer 171c is formed with the 1st conductive ingredient layer formation process on the 1st aforementioned insulating layer 151, through tube 4a, and the component electrode 4. If a thin film can be formed and a fine pattern can be formed, various kinds of processing approaches, such as plating, sputtering, and vacuum evaporationo, can be freely chosen as formation of

this 1st conductive ingredient layer 171c.
[0045] Next, at a plastic surgery process, from said 1st conductivity ingredient layer 171c, it etches by leaving a required part and the 1st wiring 161 and the external electrode 171 are formed. Of course, the plastic surgery approach can also be chosen freely.
[0046] Next, 2nd insulating-layer 152a is formed in the front face of the 1st insulating layer 151, the 1st wiring 161, and the external electrode 171 by the photosensitive insulating material with the 2nd insulation layer forming process. As for a photosensitive insulating material, it is desirable that it is epoxy system resin. Formation of 2nd insulating-layer 151a may print a liquefied thing, and may make a film-like thing adhere.
[0047] Next, at exposure / development process, it exposes, and by developing negatives, through tube 171a is prepared on the external electrode 171, and the 2nd insulating layer 152 is formed.
[0048] In drawing 4 , although it seems that mutual spacing of two or more external electrodes 171 is narrow, as shown in drawing 2 , it is arrangement of the shape of a grid which is perpendicularly separated in space in fact.
[0049] Depending on the case, even the n-th wiring layer formation process and the n-th insulation layer forming process are repeatedly made into multilayer structure. In that case, components, such as resistance and capacity, can be added to each wiring layer. And the insulating material used above has a desirable ingredient with the middle coefficient of thermal expansion of the coefficient of thermal expansion of a semiconductor device, and the coefficient of thermal expansion of the circuit board, as shown in Table 1.
[0050]
[Table 1]

素 材	熱膨張係数 (10^{-6}/ ℃)
半導体素子	2．4
絶縁層	3～6
回路基板 (アルミナ基板)	7

[0051] In addition, although it is drawing which performs a wiring layer formation process and an insulation layer forming process after dividing a semiconductor device wafer in drawing 4 used for explanation of an example, since the semiconductor device of the whole wafer is put in block and the n-th wiring layer formation process and the n-th insulation layer forming process can be processed in the condition before division of a semiconductor device wafer, working efficiency improves very greatly.
[0052] Moreover, since a wiring layer formation process and an insulation layer forming process are the repeats of the production process of a semiconductor device, and the same process, and the thing equivalent to the manufacture track record of a semiconductor device is possible for such process tolerance, corresponding to the electrode made [overly] detailed or its pitch, manufacture of the semiconductor device of high quality is possible for it.
[0053] The process of this invention and the conventional example is compared based on drawing 5 .
[0054] In drawing 5 , although the right-hand side conventional example is as explanation of the above In the case of left-hand side this invention, the n-th wiring layer formation process and the n-th insulation layer forming process in the condition before division of a semiconductor device wafer Since the semiconductor device of the whole wafer can be processed collectively, after dividing a semiconductor device wafer, as compared with forming a bump, working efficiency improves extremely for every electrodes of those for every sheet of every of a semiconductor device in the conventional example.
[0055]
[Effect of the Invention] By the semiconductor device and its manufacture approach of this invention, since a wiring layer formation process and an insulation layer forming process are both the repeats of

the production process of a semiconductor device, and the same process, it can respond to the electrode of the semiconductor device made [overly] detailed, or its pitch, and the effectiveness that the semiconductor device of high quality can be manufactured is done so.

[0056] Moreover, in this invention, since the process of the conventional technique which requires the time amount of attaching a bump for every electrode of a semiconductor device is lost, it bundles up for every semiconductor device, it bundles up for every wafer further and inter-electrode junction is carried out, the effectiveness that productivity can be improved very greatly is done so.

[0057] Moreover, by using the insulating material which has the middle coefficient of thermal expansion of the coefficient of thermal expansion of a semiconductor device, and the coefficient of thermal expansion of the circuit board in the insulating material to be used, the thermal stress generated according to the difference of thermal expansion is eased, and the effectiveness that dependability can be improved is done so.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional side elevation showing the configuration of the 1st example of the semiconductor device of this invention.

[Drawing 2] It is the top view showing the configuration of the 1st example of the semiconductor device of this invention.

[Drawing 3] It is the sectional side elevation showing the configuration of the 2nd example of the semiconductor device of this invention.

[Drawing 4] It is process drawing showing one example of the manufacture approach of the semiconductor device of this invention.

[Drawing 5] It is drawing which compares the process of this invention and the conventional example.

[Drawing 6] It is the sectional side elevation showing the configuration and operation of a semiconductor device of the 1st conventional example.

[Drawing 7] It is the sectional side elevation showing the configuration and operation of a semiconductor device of the 1st conventional example.

[Drawing 8] It is the sectional side elevation showing the configuration of the semiconductor device of the 2nd conventional example.

[Description of Notations]

1 Semiconductor Device
1a Semiconductor device
2 Semiconductor Device
4 Component Electrode

4a Through-tube
17 Mask
18 Exposure
151 1st Insulating Layer
151a The 1st insulating layer
152 2nd Insulating Layer
152a The 2nd insulating layer
153 3rd Insulating Layer
161 1st Wiring
161a The 1st connection electrode
161b Through tube
162 2nd Wiring
171 External Electrode
171a Through tube

[Translation done.]

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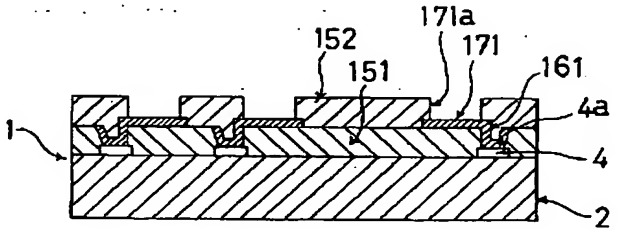
(54)【発明の名称】　半導体装置とその製造方法

(57)【要約】

【目的】　半導体素子の素子電極数が多くなり、半導体素子の素子電極が小さくなり、電極ピッチが狭くなっても、高品質の製品を生産性良く製造できる半導体装置の提供。

【構成】　集積回路が形成され複数の素子電極４を有する半導体素子２と、前記半導体素子２の表面に形成された第１絶縁層１５１と、前記第１絶縁層１５１の上に形成された複数の外部電極１７１と、前記外部電極１７１と前記素子電極４とを電気的に接続する第１配線１６１とからなる第１導電層１６１、１７１とを有する。



1……半導体装置
2……半導体素子
4……素子電極
4a……貫通孔
151……第１絶縁層
152……第２絶縁層
161……第１配線
171……外部電極
171a……貫通孔

1

【特許請求の範囲】

【請求項１】　集積回路が形成され複数の素子電極を有する半導体素子と、前記半導体素子の表面に形成された第１絶縁層と、前記第１絶縁層の上に形成された複数の外部電極と、前記外部電極と前記素子電極とを電気的に接続する第１配線とからなる第１導電層とを有することを特徴とする半導体装置。

【請求項２】　集積回路が形成され複数の素子電極を有する半導体素子と、前記半導体素子の表面に形成された第１絶縁層と、前記第１絶縁層の上に形成され前記素子電極と電気的に接続された第１配線からなる第１導電層と、前記第１導電層の上に形成された第２絶縁層と、前記第２絶縁層の上に形成された複数の外部電極と、前記外部電極と前記第１配線または前記素子電極とを電気的に接続する第２配線とからなる第２導電層とを有することを特徴とする半導体装置。

【請求項３】　半導体素子の表面に絶縁層と導電層とが繰り返し形成された多層配線構造を有し、前記多層配線構造を介して前記半導体素子の素子電極と電気的に接続された外部電極が最表面に形成されている請求項２に記載の半導体装置。

【請求項４】　絶縁層の絶縁材料の熱膨張係数は、半導体素子の熱膨張係数と回路基板の熱膨張係数との中間の値である請求項１、２又は３に記載の半導体装置。

【請求項５】　絶縁層の絶縁材料は感光性のエポキシ樹脂である請求項１、２、３又は４に記載の半導体装置。

【請求項６】　集積回路が形成され複数の素子電極を有する半導体素子の表面に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記素子電極に対する貫通孔を有する第１絶縁層を設ける第１絶縁層形成工程と、前記第１絶縁層の上に導電性材料による導電層を形成し、整形して複数の外部電極と、前記外部電極と前記素子電極とを電気的に接続する第１配線とからなる第１導電層を設ける第１導電層形成工程とを有することを特徴とする半導体装置の製造方法。

【請求項７】　集積回路が形成され複数の素子電極を有する半導体素子の表面に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記素子電極に対する貫通孔を有する第１絶縁層を設ける第１絶縁層形成工程と、前記第１絶縁層の上に導電性材料による導電層を形成し、整形して前記素子電極に接続する第１配線を有する第１導電層を設ける第１導電層形成工程と、前記第１導電層の上に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記第１配線に対する貫通孔を有する第２絶縁層を設ける第２絶縁層形成工程と、前記第２絶縁層の上に導電性材料による導電層を形成し、整形して複数の外部電極と、前記外部電極と前記第１配線または前記素子電極とを電気的に接続する第２配線とからなる第２導電層を設ける第２導電層形成工程とを有することを特徴とする半導体装置

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の製造方法。

【請求項８】　半導体素子の表面に絶縁層形成工程と導電層形成工程とを繰り返して、多層配線構造を設け、前記多層配線構造を介して半導体素子の素子電極と電気的に接続される外部電極を最表面に設ける請求項７に記載の半導体装置の製造方法。

【請求項９】　ウエハーの状態の複数の半導体素子に、絶縁層形成工程と導電層形成工程とを施す請求項６、７又は８に記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、半導体素子を半導体キャリアに高密度に実装した半導体装置とその製造方法に関するものである。

【０００２】

【従来の技術】回路基板に高密度に実装する従来の半導体装置を図５～図８に基づいて説明する。

【０００３】従来から、半導体素子２を回路基板１２に実装する場合、図６に示すように、半導体素子２を、一旦、半導体キャリア３に接続して半導体装置１とした後に、回路基板１２に接続している。これには、次の２つの理由がある。

【０００４】第１の理由は、ベア半導体素子のままでは、傷が付き易くて実装前に検査ができない。従って、実装前に検査が行えるようにし、且つ、湿度による特性劣化を防ぐために、半導体素子２を半導体キャリア３に装着し、周辺をエポキシ系樹脂の封止剤７で充填被覆している。

【０００５】第２の理由は、ベア半導体素子は、構成上、素子電極位置がベア半導体素子の周辺部に偏りスペースが限られ、スペースが限られたこれらの素子電極４は、小さくて電極間距離が狭い。そのために、前記素子電極４を回路基板１２の基板電極１１に直接に接続するのが困難である。

【０００６】この接続を容易にするために、片面の素子側電極６の配置が半導体素子２の素子電極４への接続に適し、反対面の基板側電極８の配置が回路基板１２の基板電極１１への接続に適した半導体キャリア３の前記片面に、半導体素子２を接続し、前記の理由で、その周辺をエポキシ系樹脂の封止剤７で充填被覆している。

【０００７】従って、第１従来例では、図６において、半導体装置１は、半導体素子２の素子電極４を、その上に金のバンプ５を設けクリーム半田または導電性接着剤によって、半導体キャリア３の素子側電極６に接続し、接続した半導体素子２と半導体キャリア３間の隙間および接続した半導体素子２の周辺部をエポキシ系樹脂の封止剤７で充填被覆したものである。そして、前記素子側電極６と前記基板側電極８との間は電気的に接続されている。

【０００８】半導体装置１を回路基板１２に接続する場

合には、先ず図６に示すように、半導体キャリア３の前記基板側電極８にバンプ９を設け、回路基板１２の基板電極１１にクリーム半田１３を印刷する。

【０００９】次いで、図７に示すように、半導体装置１の基板側電極８を、回路基板１２の基板電極１１上に位置決めして載置し、加熱して前記塗布されたクリーム半田１３を溶融・硬化して、基板側電極８を基板電極１１に接続する。

【００１０】次に、第２従来例を図８に基づいて説明する。

【００１１】図８において、半導体装置１は、半導体素子２の複数の素子電極４の上に金のバンプ５を形成し、前記金のバンプ５を導電性接着剤５ａによってポリイミドフイルム１４上に形成された素子側電極６に接続し、半導体素子２とポリイミドフイルム１４との間隙にはエポキシ系樹脂の封止剤７が充填されている。そして、素子側電極６にバンプ９を設け、これを回路基板の電極に接続する。図８は断面を示すものであるが、実際には、半導体素子２の周辺部に偏っている多数の素子電極４が紙面に垂直方向に密に配置されており、素子側電極６は、半導体素子２の中央部の広いスペースに格子状に配置されている。

【００１２】

【発明が解決しようとする課題】しかし、上記の従来例の構成では、半導体素子のウエハーから半導体装置として出荷するまでの工程が、図５に示すように、分割工程で、半導体素子のウエハーを一つ一つの半導体素子に分割し、バンプ形成工程で、一つ一つの半導体素子に対してその素子電極の数だけのバンプ形成を繰り返し、位置決め・接合工程で、バンプ形成が終了した半導体素子を、半導体キャリアに一つ一つ位置決め・接合する必要がある。

【００１３】従って、最近のように半導体素子の素子電極の数が多くなると生産工程に非常に時間がかかるという問題点がある。

【００１４】又図６、図７に示す封止剤７の硬化工程にも長時間を要するという問題点がある。

【００１５】又、半導体キャリア３に求められる特性として、その平坦度は、電極接合強度の信頼性を維持するために、反り量が１０μｍ以下、基板側電極の大きさは１００μｍ×１００μｍ以上であり、反り量が１０μｍを越えると電極接合不良が発生し、基板側電極の面積が不足したり、ピッチが狭くなり過ぎると、高品質の製造が困難になり、ブリッジ等の不良が発生するという問題点がある。

【００１６】本発明は、上記の問題点を解決し、半導体素子の素子電極数が多くなり、半導体素子の素子電極が小さくなり、電極ピッチが狭くなっても、高品質の製品を生産性良く製造できる半導体装置とその製造方法を提供することを課題とする。

【００１７】

【課題を解決するための手段】本願第１発明の半導体装置は、上記の課題を解決するために、集積回路が形成され複数の素子電極を有する半導体素子と、前記半導体素子の表面に形成された第１絶縁層と、前記第１絶縁層の上に形成された複数の外部電極と、前記外部電極と前記素子電極とを電気的に接続する第１配線とからなる第１導電層とを有することを特徴とする。

【００１８】本願第２発明の半導体装置は、上記の課題を解決するために、集積回路が形成され複数の素子電極を有する半導体素子と、前記半導体素子の表面に形成された第１絶縁層と、前記第１絶縁層の上に形成され前記素子電極と電気的に接続された第１配線からなる第１導電層と、前記第１導電層の上に形成された第２絶縁層と、前記第２絶縁層の上に形成された複数の外部電極と、前記外部電極と前記第１配線または前記素子電極とを電気的に接続する第２配線とからなる第２導電層とを有することを特徴とする。

【００１９】又、本願第２発明の半導体装置は、上記の課題を解決するために、半導体素子の表面に絶縁層と導電層とが繰り返し形成された多層配線構造を有し、前記多層配線構造を介して前記半導体素子の素子電極と電気的に接続された外部電極が最表面に形成されていることが好適である。

【００２０】又、本願第１、第２又は第３発明の半導体装置は、上記の課題を解決するために、絶縁層の絶縁材料の熱膨張係数は、半導体素子の熱膨張係数と回路基板の熱膨張係数との中間の値であることが好適である。

【００２１】又、本願第１、第２、第３又は第４発明の半導体装置は、上記の課題を解決するために、絶縁層の絶縁材料は感光性のエポキシ樹脂であることが好適である。

【００２２】本願第３発明の半導体装置の製造方法は、上記の課題を解決するために、集積回路が形成され複数の素子電極を有する半導体素子の表面に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記素子電極に対する貫通孔を有する第１絶縁層を設ける第１絶縁層形成工程と、前記第１絶縁層の上に導電性材料による導電層を形成し、整形して複数の外部電極と、前記外部電極と前記素子電極とを電気的に接続する第１配線とからなる第１導電層を設ける第１導電層形成工程とを有することを特徴とする。

【００２３】本願第４発明の半導体装置の製造方法は、上記の課題を解決するために、集積回路が形成され複数の素子電極を有する半導体素子の表面に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記素子電極に対する貫通孔を有する第１絶縁層を設ける第１絶縁層形成工程と、前記第１絶縁層の上に導電性材料による導電層を形成し、整形して前記素子電極に接続する第１配線を有する第１導電層を設ける第１

導電層形成工程と、前記第１導電層の上に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記第１配線に対する貫通孔を有する第２絶縁層を設ける第２絶縁層形成工程と、前記第２絶縁層の上に導電性材料による導電層を形成し、整形して複数の外部電極と、前記外部電極と前記第１配線または前記素子電極とを電気的に接続する第２配線とからなる第２導電層を設ける第２導電層形成工程とを有することを特徴とする。

【００２４】又、本願第４発明の半導体装置の製造方法は、上記の課題を解決するために、半導体素子の表面に絶縁層形成工程と導電層形成工程とを繰り返して多層配線構造を設け、最表面に前記多層配線構造を介して半導体素子の素子電極と電気的に接続される外部電極を設けることが好適である。

【００２５】又、本願第３又は第４発明の半導体装置の製造方法は、上記の課題を解決するために、ウエハーの状態の複数の半導体素子に、絶縁層形成工程と導電層形成工程とを施すことが好適である。

【００２６】

【作用】本願発明の半導体装置と、本願発明の半導体装置の製造方法とは、集積回路が形成され複数の素子電極を有する半導体素子の表面に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記素子電極に対する貫通孔を有する第１絶縁層を設ける第１絶縁層形成工程と、前記第１絶縁層の上に導電性材料による導電層を形成し、整形して前記素子電極に接続する第１配線を有する第１導電層を設ける第１導電層形成工程との組合せによるものであり、これらの工程は半導体素子の製造技術の実績を利用できるので、超微細化される半導体素子の素子電極やそのピッチに対応して、高品質な半導体装置を得ることができる。

【００２７】又、半導体素子の各素子電極毎にバンプを取り付けるという時間がかかる従来技術の工程が無くなり、各半導体素子毎に一括して、更に、各ウエハーごとに一括して素子電極と外部電極間の電極接合を行うので、生産性を極めて大きく向上できる。

【００２８】又、使用する絶縁材料に、半導体素子の熱膨張係数と回路基板の熱膨張係数との中間の熱膨張係数を持つ絶縁材料を使用することによって、熱膨張の差によって発生する熱応力を緩和し信頼性を向上できる。

【００２９】

【実施例】本発明の半導体装置の第１実施例を図１、図２に基づいて説明する。

【００３０】図１、図２において、本実施例の半導体装置１の構造は、複数の素子電極４を有する半導体素子２上に第１絶縁層１５１が形成されており、素子電極４の上には、貫通孔４ａが設けられている。第１絶縁層１５１の上には第１配線１６１と第１外部電極１７１とが設けられ、第１配線１６１は第１外部電極１７１と素子電極４とを接続している。第１絶縁層１５１と第１配線１６１と第１外部電極１７１との上には、第２絶縁層１５２が設けられ、第１外部電極１７１の上には貫通孔１７１ａが開けられている。この第１外部電極１７１が本実施例の半導体素子１の外部電極になる。

【００３１】そして、素子電極４は、図２に示すように、半導体素子２の構成によって、半導体素子２の周辺部に偏って配置されているので、半導体素子２が小型化され、且つ、素子電極４の数が多くなると、素子電極４の面積が小さくなり、電極間ピッチが狭くなるが、第１外部電極１７１は、半導体素子２の中央部の広いスペースに配置され、形、面積、配置の制限が少なく、図２に示すように、回路基板の基板電極に接続し易い配置に、例えば、格子状等の配置に自由に設計できる。

【００３２】本発明の半導体装置の第２実施例を図３に基づいて説明する。

【００３３】図３において、本実施例の半導体装置１ａの構造は、第１実施例の構造を多層構造にしたものである。

【００３４】複数の素子電極４を有する半導体素子２上に第１絶縁層１５１が形成されており、素子電極４の上には、貫通孔４ａが設けられている。

【００３５】第１絶縁層１５１の上には第１配線１６１と第１接続電極１６１ａとが設けられ、第１配線１６１は素子電極４と第１接続電極１６１ａとに接続している。

【００３６】第１絶縁層１５１と第１配線１６１と第１接続電極１６１ａとの上には、第２絶縁層１５２が設けられ、第１接続電極１６１ａの上には貫通孔１６１ｂが設けられている。

【００３７】第２絶縁層１５２の上には第２配線１６２と第２外部電極１７２とが設けられ、第２配線１６２は第１接続電極１６１ａに接続している。

【００３８】第２絶縁層１５２と第２配線１６２と第２外部電極１７２との上には、第３絶縁層１５３が設けられ、第２外部電極１７２の上には貫通孔１７２ａが設けられている。

【００３９】上記の多層構造は、２層に限らず、何層でも可能であり、これらの層の配線部に、抵抗、容量等の回路素子の付加を設計することができる。

【００４０】本発明の半導体装置の製造方法を図４、図５に基づいて説明する。

【００４１】図４において、先ず、第１の絶縁層形成工程で、素子電極４を有する半導体素子２の表面に感光性絶縁材料で第１の絶縁層１５１ａを形成する。感光性絶縁材料はエポキシ系樹脂であることが好ましい。第１の絶縁層１５１ａの形成は、液状のものを印刷しても良く、フイルム状のものを付着させても良い。

【００４２】次に、露光工程で、所定パターンの光が通過するように形成されたマスク１７を使用して露光１８

する。

【００４３】次に、現像工程で、現像することによって、素子電極４の上に貫通孔４ａを設け、第１絶縁層１５１を形成する。

【００４４】次に、第１の導電性材料層形成工程で、前記の第１絶縁層１５１と貫通孔４ａと素子電極４との上に、第１の導電性材料層１７１ｃを形成する。この第１の導電性材料層１７１ｃの形成には、薄膜を形成することができ、ファインパターンを形成できるものであれば、メッキ、スパッタリング、蒸着等の各種の加工方法を自由に選択できる。

【００４５】次に、整形工程で、前記第１導電性材料層１７１ｃから、必要な部分を残して、エッチングを行い、第１配線１６１と外部電極１７１とを形成する。勿論、整形方法も自由に選択できる。

【００４６】次に、第２の絶縁層形成工程で、第１絶縁層１５１と第１配線１６１と外部電極１７１との表面に感光性絶縁材料で第２の絶縁層１５２ａを形成する。感光性絶縁材料はエポキシ系樹脂であることが好ましい。第２の絶縁層１５１ａの形成は、液状のものを印刷しても良く、フイルム状のものを付着させても良い。

【００４７】次に、露光・現像工程で、露光し、現像することによって、外部電極１７１の上に貫通孔１７１ａを設け、第２絶縁層１５２を形成する。

【００４８】図４において、複数の外部電極１７１の相互間隔が狭くなっているように見えるが、実際には、例えば、図２に示すように、紙面に垂直方向に離れている格子状の配置である。

【００４９】場合によっては、第ｎ配線層形成工程、第ｎ絶縁層形成工程までを繰り返して多層構造にする。その際に、各配線層に抵抗、容量等の素子を付加できる。そして、上記に使用する絶縁材料は、表１に示すように、半導体素子の熱膨張係数と回路基板の熱膨張係数との中間の熱膨張係数を持つ材料が好ましい。

【００５０】

【表１】

素　材	熱膨張係数 (10^{-6}/℃)
半導体素子	2．4
絶縁層	3～6
回路基板（アルミナ基板）	7

【００５１】尚、実施例の説明に使用した図４では、配線層形成工程と絶縁層形成工程とを、半導体素子ウエハーを分割した後に行うような図になっているが、第ｎ配線層形成工程、第ｎ絶縁層形成工程を、半導体素子ウエハーの分割前の状態で、そのウエハー全体の半導体素子を一括して処理できるので、作業効率が極めて大きく向上する。

【００５２】又、配線層形成工程と絶縁層形成工程とは、半導体素子の製造工程と同様の工程の繰り返しであるので、これらの加工精度は、半導体素子の製造実績と同等のものが可能であるから、超微細化される電極やそのピッチに対応して、高品質の半導体装置の製造が可能である。

【００５３】図５に基づいて、本発明と従来例との工程を比較する。

【００５４】図５において、右側の従来例は前記の説明の通りであるが、左側の本発明の場合には、第ｎ配線層形成工程と第ｎ絶縁層形成工程とを、半導体素子ウエハーの分割前の状態で、そのウエハー全体の半導体素子を一括して処理できるので、従来例で、半導体素子ウエハーを分割してから、半導体素子の一枚一枚毎に、それらの各電極毎に、バンプを形成するのに比較して、作業効率が極めて向上する。

【００５５】

【発明の効果】本発明の半導体装置とその製造方法では、配線層形成工程と絶縁層形成工程とが共に、半導体素子の製造工程と同様の工程の繰り返しであるので、超微細化される半導体素子の電極やそのピッチに対応することができ、高品質の半導体装置を製造できるという効果を奏する。

【００５６】又、本発明では、半導体素子の各電極毎にバンプを取り付けるという時間がかかる従来技術の工程が無くなり、各半導体素子毎に一括して、更に、各ウエハーごとに一括して電極間接合するので、生産性を極めて大きく向上できるという効果を奏する。

【００５７】又、使用する絶縁材料に、半導体素子の熱膨張係数と回路基板の熱膨張係数との中間の熱膨張係数を持つ絶縁材料を使用することによって、熱膨張の差によって発生する熱応力を緩和し信頼性を向上できるという効果を奏する。

【図面の簡単な説明】

【図１】本発明の半導体装置の第１実施例の構成を示す側断面図である。

【図２】本発明の半導体装置の第１実施例の構成を示す平面図である。

【図３】本発明の半導体装置の第２実施例の構成を示す側断面図である。

【図４】本発明の半導体装置の製造方法の一実施例を示す工程図である。

【図５】本発明と従来例との工程を比較する図である。

【図６】第１従来例の半導体装置の構成と使用方法とを示す側断面図である。

【図７】第１従来例の半導体装置の構成と使用方法とを示す側断面図である。

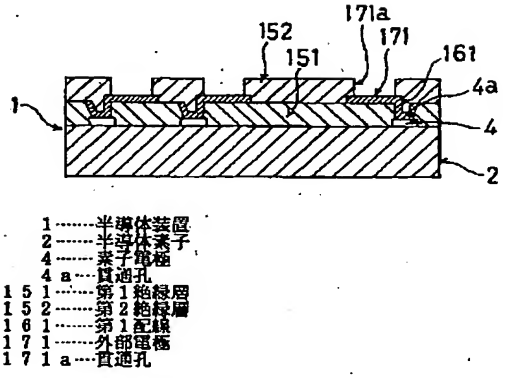
【図８】第２従来例の半導体装置の構成を示す側断面図である。

【符号の説明】

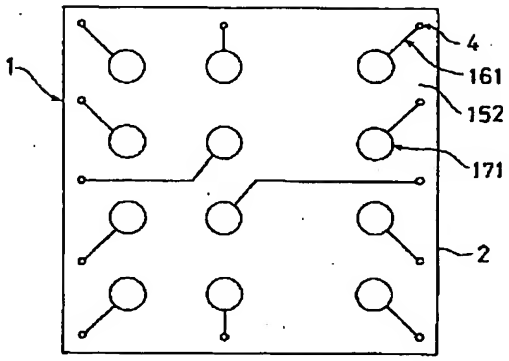
1　半導体装置
1a　半導体装置
2　半導体素子
4　素子電極
4a　貫通孔
17　マスク
18　露光
151　第1絶縁層
151a　第1の絶縁層

152　第2絶縁層
152a　第2の絶縁層
153　第3絶縁層
161　第1配線
161a　第1接続電極
161b　貫通孔
162　第2配線
171　外部電極
171a　貫通孔

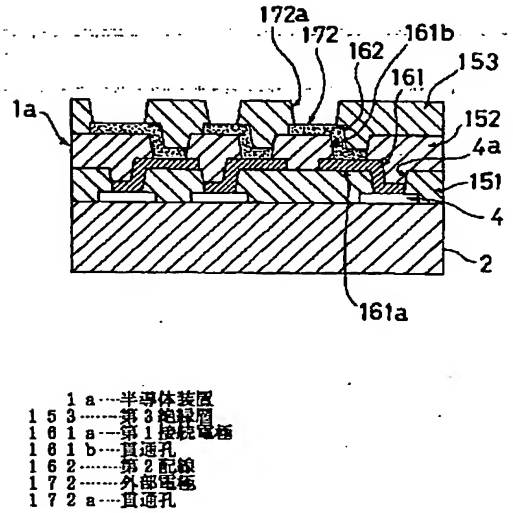
【図1】



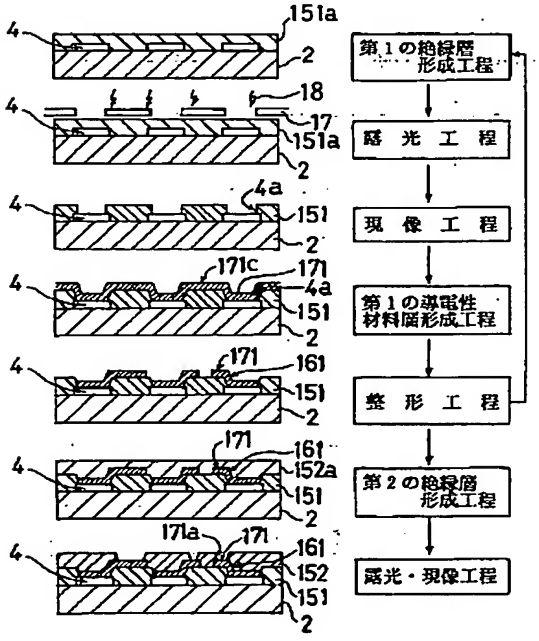
【図2】



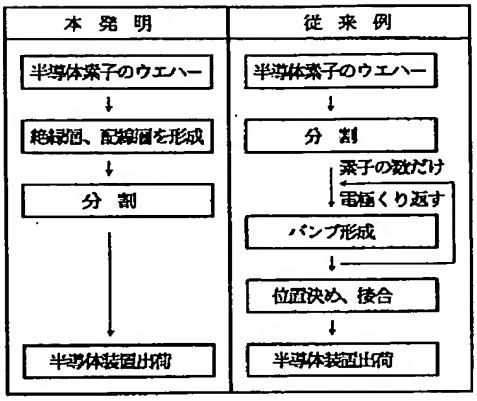
【図3】



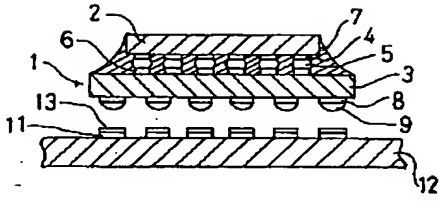
【図4】



【図５】


本発明
従来例
半導体素子のウエハー
絶縁膜、配線層を形成
分割
半導体装置出荷
半導体素子のウエハー
分割
素子の数だけ
電極くり返す
バンプ形成
位置決め、接合
半導体装置出荷

【図６】


2
7
6
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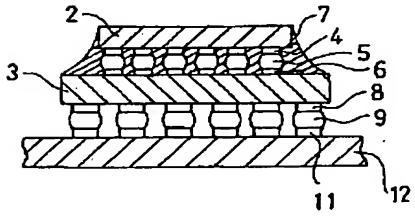
12

【図７】


2
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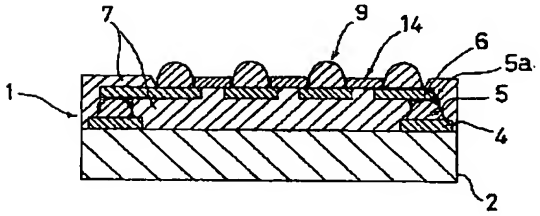
12

【図８】


7
9
14
6
5a
1
5
4
2